

Remarks

Entry of the above-noted amendments, reconsideration of the application, and allowance of all claims pending are respectfully requested. By this amendment, claims 1, 4, and 13 are amended and claims 3, 21, and 22 are canceled. These amendments to the claims constitute a bona fide attempt by applicant to advance prosecution of the application and obtain allowance of certain claims, and are in no way meant to acquiesce to the substance of the rejections. Support for the amendments can be found throughout the specification (e.g., page 3, lines 21-31; page 7, lines 18-31), figures (e.g., FIG. 1), and claims (e.g., previously presented claims 3, 21, and 22) and thus, no new matter has been added. Claims 1-2, 4-6, 8-16, and 18-20 are pending.

Claim Rejections - 35 U.S.C. § 103

Claim 1 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis ("The Transmogrifier-2: A Million Gate Rapid-Prototyping System"; IEEE Transactions on Very Large Scale Integration Systems; June 1998) in view of FLEX10K ("FLEX 10K Device Family"; web.archive.org/20000303160208/www.altera.com/html/products/f10k.html; March 2000) and further in view of Brynjolfson ("Dynamic Clock Management for Low Power Applications in FPGAs"; Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 21-24 May 2000; pages 139-142). Claim 2 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis, FLEX10K, and Brynjolfson in view of Mitchell (U.S. Patent No. 6,230,119). Claim 3 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis, FLEX10K, and Brynjolfson in view of Keenan et al. (U.S. Patent No. 4,903,199; "Keenan"). Claims 4 and 21 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis, Mitchell, and Brynjolfson and further in view of Keenan. Claims 5 and 8-12 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis,

Keenan, Mitchell, and Brynjolfson in view of common knowledge in the art. Claim 6 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis, Keenan, and Brynjolfson in view of Wray ("Using microprocessors and microcomputers: the Motorola family"; 1994) and further in view of common knowledge in the art. Claims 13 and 22 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis and Brynjolfson in view of Keenan. Claims 14-15 and 18-20 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis, Keenan, and Brynjolfson in view of common knowledge in the art. Claim 16 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lewis, Keenan, and Brynjolfson in view of Wray, further in view of common knowledge in the art.

These rejections are respectfully, but most strenuously, traversed.

Applicant notes that while some of the cited references disclose emulation of processor operations, the cited references fail to disclose repeated emulation of processor operations without interruption from other cyclical processor operations of the processor. Referring to page 2, lines 1-19 of the present application, processor emulators of the prior art emulate all operations of the processor as exactly as possible. In addition, emulators imitate the operational cycles of the processor. For example, when a processor utilizes a RISC (Reduced Instruction Set Computing) architecture, the processor alternates between the various operations that it provides, often leaving an operation before it is completed in order to perform another task prior to returning to the incomplete operation. In normal operation, such activity is not a problem because the speed of the processor is so fast that such interruptions are not noticeable to the user. When trying to debug a test circuit, however, such interruptions may delay the ability to test a particular operation because of the need to wait for the processor or its emulator to cycle back to a particular operation.

Applicant respectfully submits that the Office Action's citations to the applied references, with or without modification or combination, assuming, *arguendo*, that the modification or combination of the Office Action's citations to the applied references is proper, do not teach or suggest that the programmable logic device is arranged and constructed to emulate the at least one processor operation repeatedly **without interruption from the one or more cyclical processor operations** other than the at least one operation of the processor, as recited in applicant's independent claim 1.

For explanatory purposes, applicant discusses herein one or more differences between the claimed invention and the Office Action's citations to Lewis, Flex10K, Brynjolfson, Mitchell, Keenan, and Wray. This discussion, however, is in no way meant to acquiesce in any characterization that one or more parts of the Office Action's citations to Lewis, Flex10K, Brynjolfson, Mitchell, Keenan, and Wray correspond to the claimed invention.

Lewis (Abstract, lines 1-17) discloses a multifield programmable gate array rapid-prototyping system. Lewis (page 188, column 1, lines 11-15; column 2, lines 11-15) discloses:

A number of field-programmable systems have been described [1]-[7], and can be roughly classified either as emulation systems, or custom compute engines. Emulation systems tend to be targeted at emulating ASIC's, which can be designed for a wide range of applications...

By designing with the TM-2 as a target, it is hoped that higher utilization than emulation engines can be attained, while with the inclusion of a flexible routing structure it is hoped to be possible to accommodate a wider range of applications than computer engines.

Lewis fails to disclose that the programmable logic device is arranged and constructed to emulate the at least one processor operation repeatedly without interruption from the one or more cyclical processor operations other than the at least one operation of the processor. This point has been conceded by the Office Action (sections 6.5, 7.6.1, 7.17, 8.4, 10.5.1, 10.13, and 11.6).

So, the Office Action's citation to Lewis fails to satisfy at least one of the limitations recited in applicant's independent claim 1.

Flex10K (section: "Embedded Array Revolutionizes Programmable Logic") discloses the Flex10K device family of field programmable gate arrays. Flex10K fails to disclose emulation of at least one processor operation repeatedly without interruption from one or more cyclical processor operations other than the at least one operation of the processor.

So, the Office Action's citation to Flex10K fails to satisfy at least one of the limitations recited in applicant's independent claim 1.

Brynjolfson (Abstract) discloses dynamically controlled clock rates. Brynjolfson fails to disclose emulation of at least one processor operation repeatedly without interruption from one or more cyclical processor operations other than the at least one operation of the processor.

So, the Office Action's citation to Brynjolfson fails to satisfy at least one of the limitations recited in applicant's independent claim 1.

Mitchell (column 2, line 58 to column 3, line 2) discloses:

Preferably the emulator is a software controlled emulator, and comprises emulation instructions held as software within a reserved memory integrated into the data processor. The receipt of the instruction to start emulation, either by a signal on the emulator control pin or via a software instruction within the software being debugged, forces the data processing core of the data processor to suspend execution of the user's programming code and to execute instructions from the emulation instruction code. Preferably the receipt of an instruction to commence emulation causes a high level non maskable interrupt to be issued to the data processing core of the data processor. (emphasis added)

Mitchell discloses emulation of a processor with interruptions to the data processing core. Mitchell fails to disclose emulation of at least one processor operation repeatedly without interruption from one or more cyclical processor operations other than the at least one operation of the processor.

So, the Office Action's citation to Mitchell fails to satisfy at least one of the limitations recited in applicant's independent claim 1.

Keenan (column 1, lines 47-57; column 2, lines 25-30; column 6, lines 24-30) discloses testing integrated circuits using an interpreted language (such as BASIC). Keenan is directed towards speeding up execution of software programs. The software programs operate at a higher level than the processor operations of the present invention. Keenan (column 4, lines 47-63) discloses that a single program statement is converted to a short assembly language loop. Applicant notes that processor operations (such as those disclosed by Wray, pages 646-647) cannot be broken down into smaller statements. So, the single test loop disclosed by Keenan cannot correspond to the at least one processor operation. Keenan fails to disclose emulation of at least one processor operation repeatedly without interruption from one or more cyclical processor operations other than the at least one operation of the processor.

So, the Office Action's citation to Keenan fails to satisfy at least one of the limitations recited in applicant's independent claim 1.

Wray (page 346, lines 2-5) discloses testing procedures for microprocessors. Wray fails to disclose emulation of at least one processor operation repeatedly without interruption from one or more cyclical processor operations other than the at least one operation of the processor.

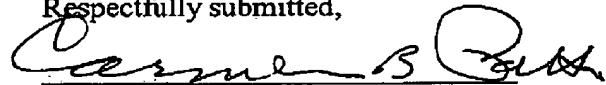
So, the Office Action's citation to Wray fails to satisfy at least one of the limitations recited in applicant's independent claim 1.

For all the reasons presented above with reference to claim 1, claims 1, 4, and 13 are believed neither anticipated nor obvious over the art of record. The corresponding dependent claims are believed allowable for the same reasons as independent claims 1, 4, and 13, as well as for their own additional characterizations.

Withdrawal of the § 103 rejections is therefore respectfully requested.

In view of the above amendments and remarks, allowance of all claims pending is respectfully requested. If a telephone conference would be of assistance in advancing the prosecution of this application, the Examiner is invited to call applicant's attorney.

Respectfully submitted,


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